## IN THE CLAIMS

1. (Currently Amended) A programmable element, comprising:

a first source/drain region, a second source/drain region and a conduction channel between the first source/drain region and the second source/drain region, and having a gate isolated from the conduction channel by a gate oxide; and

the gate oxide having an electron charge trapped in the gate oxide adjacent to the first source/drain region and substantially no charge trapped in the gate oxide adjacent to the second source/drain region, the amount of electron charge trapped in the gate oxide adjacent to the first source/drain region is sufficient to cause the conduction channel to have at ~~lease~~ least two different voltage threshold regions.

2. (Original) The programmable element of claim 1 further including programming circuitry to inject electrons into the gate oxide and erase circuitry to remove electrons from the gate oxide.

3. (Original) The programmable element of claim 1 further including programming circuitry to inject electrons into the gate oxide and read circuitry to sense injected electrons in the gate oxide.

4. (Original) The programmable element of claim 1 further including programming circuitry to apply a positive voltage potential between the first source/drain region (V1) and the second source/drain region (V2) where V1 is greater than V2, to inject electrons into the gate oxide nearest the first source /drain region.

5. (Original) The programmable element of claim 1 further including read circuitry to apply a positive voltage potential between the second source/drain region (V2) and the first source/drain region (V1) where V2 is greater than V1, to sense injected electrons in the gate oxide nearest the first source/drain region.

6. (Original) The programmable element of claim 1 wherein the current through the second source/drain region is less in a programmed state than the current through the second source/drain region in an un-programmed state.

7. (Original) A non-volatile memory, comprising:

a programmable element having a first source/drain region, a second source/drain region and a conduction channel between the first source/drain region and the second source/drain region, and having a gate isolated from the conduction channel by a gate oxide, the gate oxide having an electron charge trapped in the gate oxide adjacent to the first source/drain region and substantially no charge trapped in the gate oxide adjacent to the second source/drain region, the amount of the electron charge trapped in the gate oxide causes the conduction channel to have at least two different voltage threshold regions.

8. (Original) The non-volatile memory of claim 7 wherein programming the programmable element applies a reverse voltage to the source/drain regions and reading the programmed element applies a forward voltage between the source/drain regions.

9. (Original) The non-volatile memory of claim 7 wherein, in a programmed state, the conduction channel will have a first voltage threshold region (Vt1) adjacent to the second source/drain region and a second voltage threshold region (Vt2) adjacent to the first source/drain region.

10. (Original) The non-volatile memory of claim 9 wherein the Vt2 has a greater voltage threshold than the Vt1 due to the hot electron injection into the gate oxide adjacent to the first source/drain region.

11. (Original) The non-volatile memory of claim 7 wherein the channel region has a first voltage threshold region (Vt1) and a second voltage threshold region (Vt2).

12. (Original) A non-volatile memory cell comprising a semiconductor element having a source region, a drain region and a channel region, the channel region located between the source region and the drain region, and having a conductive gate located adjacent to and separated from the channel region by a charge trapping insulator such that the channel region has a first voltage threshold (Vt1) in a first portion of the channel and a second voltage threshold (Vt2) in a second portion of the channel region.

13. (Original) The non-volatile memory cell of claim 12 wherein the channel region programmed through hot electron injection for a second programmed state.

14. (Original) The non-volatile memory cell of claim 12 wherein the first portion of the channel region is adjacent the drain region and the second portion of the channel region is adjacent to the source region.

15. (Original) A programmable memory element, comprising:

a metal-oxide-semiconductor transistor having a source region, a drain region and a channel region between the source and drain regions, and having a gate separated from the channel region by a gate oxide;

the transistor having a first programmed state whereby electrons are injected into the gate oxide by avalanche hot electron injection; and

the transistor having a second programmed state whereby the electrons are re-emitted back into the channel region.

16. (Original) The programmable memory element of claim 15 wherein the first programmed state has an electron charge trapped in the gate oxide adjacent to the source region and substantially no charge trapped in the gate oxide adjacent to the drain region such that the channel region has a first voltage threshold region (Vt1) and a second voltage threshold region (Vt2).

17. (Original) The programmable memory element of claim 15 wherein the charge trapping element is a programmable device having a charge trapped in the gate oxide adjacent to the source region and substantially no charge trapped in the gate oxide adjacent to the drain region such that the channel region has a first voltage threshold region (Vt1) and a second voltage threshold region (Vt2).

18. (Original) A non-volatile memory, comprising:

a charge trapping element having a source region, a drain region and a channel region between the source and drain regions, and having a gate separated from the channel region by a gate oxide;

a wordline coupled to the gate;

a first line coupled to the source region;

a second line coupled to the drain region; and

wherein the charge trapping element is a programmable device having a charge trapped in the gate oxide adjacent to the source region and substantially no charge trapped in the gate oxide adjacent to the drain region such that the channel region has a first voltage threshold region (Vt1) and a second voltage threshold region (Vt2).

19. (Original) The non-volatile memory of claim 18, wherein in a read mode, the first line is a source line and the second line is a bitline.

20. (Original) The non-volatile memory of claim 19, wherein the source line is operatively coupled to the source region of the charge trapping element and the bitline is operatively coupled to the drain region of the charge trapping element.

21. (Original) The non-volatile memory of claim 18, wherein the charge trapped in the gate oxide adjacent the source region includes a trapped electron charge.

22. (Original) The non-volatile memory of claim 18, wherein the second voltage threshold region (Vt2) in the channel is adjacent the source region, the first voltage threshold region (Vt1) in the channel is adjacent the drain region wherein the Vt2 has a higher voltage threshold than the Vt1.

23. (Original) The non-volatile memory of claim 18, wherein the charge trapping element includes a non-volatile, reprogrammable metal oxide semiconductor field effect transistor (MOSFET).

24. (Original) A non-volatile reprogrammable memory, comprising:

a transistor having a source region, a drain region and a channel region located between the source region and drain region, and a gate separated from the channel region by a charge trapping gate oxide;

a wordline coupled to the gate;

a source line operatively coupled to source region;

a bitline operatively coupled to the drain region; and

wherein the transistor is a programmable device having an electron charge trapped in the gate oxide adjacent to the source region and substantially no charge trapped in the gate oxide adjacent to the drain region such that the channel region has a first voltage threshold region (Vt1) and a second voltage threshold region (Vt2), Vt2 having a higher voltage threshold than Vt1.

25. (Original) The non-volatile reprogrammable memory of claim 24, wherein the transistor is a non-volatile, reprogrammable metal oxide semiconductor field effect transistor (MOSFET).

26. (Original) A non-volatile programmable memory, comprising:

a metal-oxide-semiconductor (MOS) transistor in a substrate, the MOS transistor having a source region, a drain region, and a channel region separating the source region and the drain region, and a gate separated from the channel region by an insulating layer;

a wordline coupled to the gate;

a source line coupled to the source region;

a bitline coupled to the drain region; and

wherein the MOS transistor is a programmed MOS transistor having an electron charge trapped in the insulating layer such that the channel region has a first voltage threshold region (Vt1) adjacent to the drain region and a second voltage threshold region (Vt2) adjacent to the source region, the Vt2 having a greater voltage threshold than Vt1.

27. (Original) The non-volatile programmable memory of claim 26, wherein the transistor is a metal oxide semiconductor field effect transistor (MOSFET) which is programmed with avalanche hot electron injection to trap electrons in the gate oxide.

28. (Original) A method of programming a non-volatile memory cell, comprising:

applying a first voltage (V1) to a first source/drain terminal of a transistor;

applying a second voltage (V2) to a second source/drain terminal of the transistor, where the second voltage is greater than the first voltage;

applying a gate voltage sufficient to turn on a channel of the transistor; and

injecting electrons into a gate oxide of the transistor adjacent to the first source/drain region but not adjacent to the second source/drain region.

29. (Original) The method of claim 28 further comprises reading the non-volatile memory cell, comprising:

applying a third voltage to the first source/drain terminal of the transistor;
applying a fourth voltage to the second source/drain terminal of the transistor, where the third voltage is greater than the fourth voltage;

applying a gate voltage sufficient to turn on a channel of the transistor; and

sensing injected electrons in the gate oxide of the transistor adjacent to the first source/drain region.

30. (Original) The method of claim 28 further comprising unprogramming the transistor by applying a negative gate voltage to free the electrons trapped in the gate oxide.

31. (Original) A method of using a transistor as a non-volatile memory cell comprising operating the transistor in a reverse direction to program the transistor by avalanche hot electron injection from a channel of the transistor to trap electrons in the gate oxide adjacent to a source of the transistor resulting in a programmed transistor

32. (Original) The method of claim 31 wherein the channel of the programmed transistor has two different threshold voltage regions.

33. (Original) The method of claim 31 wherein the programmed transistor is subsequently operated in the forward direction to sense the electrons trapped in the oxide near the source.

34. (Currently Amended) The method of claim 33 ~~92~~ wherein the channel of the programmed transistor has two different threshold voltage regions.

35. (Original) The method of claim 34 wherein the channel of the programmed transistor conducts significantly less current than the programmed transistor in an unprogrammed state.

36. (Original) The method of claim 31 wherein the channel of the programmed transistor conducts significantly less current than an unprogrammed transistor at state at low drain voltages.

37. (Original) The method of claim 31 further comprising unprogramming the transistor by applying a negative gate voltage to free the electrons trapped in the gate oxide.

38. (Original) A method of utilizing a MOSFET as a memory cell comprising operating the MOSFET in a reverse direction to trap electrons in a source end of a gate oxide of the MOSFET to cause the channel to have at least two different threshold voltage regions.

39. (Original) The method of claim 38 further comprising operating the MOSFET in a forward direction to sense the electrons trapped in the oxide near the source end of the gate.

40. (Original) The method of claim 38 further comprising operating the MOSFET in a forward direction to sense the channel having the at least two different threshold voltage regions.

41. (Original) The method of claim 38 further comprising operating the MOSFET with a negative gate voltage to free the electrons trapped in the oxide near the source end of the gate.

42. (Original) A method of using a normal MOSFET as a memory cell, comprising:

programming the MOSFET by operation in the reverse direction and utilizing avalanche hot electron injection to trap electrons in the gate oxide of the MOSFET causing a channel of the MOSFET to have two different threshold voltage regions; and

reading the programmed MOSFET by operating the MOSFET in the forward direction to sense the electrons trapped in the oxide near a source of the MOSFET.

43. (Original) The method of claim 42 wherein the channel of the programmed MOSFET conducts less current than an unprogrammed MOSFET.

44. (Original) The method of claim 42 further comprising unprogramming the MOSFET by applying a negative voltage to a gate of the MOSFET in relation to the voltages applied at the source and a drain of the MOSFET.

45. (Original) The method of claim 42 wherein programming the MOSFET further comprises:

applying a first voltage to the source of the MOSFET; and

applying a second voltage to the drain of the MOSFET such that the second voltage is greater than the first voltage.

46. (Original) The method of claim 42 wherein reading the programmed MOSFET comprises:

applying a first voltage to the source of the MOSFET; and

applying a second voltage to the drain of the MOSFET such that the first voltage is greater than the second voltage.

47. (Original) The method of claim 42 wherein erasing the programmed MOSFET comprises:

applying a first voltage to the source of the MOSFET;

applying a second voltage to the drain of the MOSFET; and

applying a negative voltage to the gate such that the negative voltage is negative in relation to the first voltage and the second voltage.

48. (Original) The method of claim 47 wherein erasing further comprises re-emitting the trapped electrons from the gate oxide into the channel.

49. (Original) A method of operating a transistor as a non-volatile memory cell, comprising:

applying a first voltage to a drain terminal of the transistor;

applying a second voltage to a source terminal of the transistor, where the second voltage is greater than the first voltage;

injecting electrons from a channel of the transistor into a gate oxide of the transistor;

applying a third voltage to the drain terminal of the transistor;

applying a fourth voltage to the source terminal of the transistor, where the third voltage is greater than the fourth voltage; and

sensing the electrons trapped in the gate oxide of the transistor.

50. (Original) The method of claim 49 further comprising unprogramming the transistor by applying a negative gate voltage to free the electrons trapped in the gate oxide.

51. (Original) The method of claim 49 wherein the channel of the transistor has two different threshold voltage regions.

52. (Original) A method of operating a MOSFET as a non-volatile memory cell comprising:

operating the MOSFET in a reverse direction to trap electrons in a source end of a gate oxide of the MOSFET to cause the channel to have at least two different threshold voltage regions; and

operating the MOSFET in a forward direction to sense the trapped electrons in the source end of the gate oxide of the MOSFET.

53. (Original) The method of claim 52 wherein the channel of the programmed transistor conducts significantly less current than the programmed transistor in an unprogrammed state.

54. (Original) The method of claim 52 further comprising unprogramming the transistor by applying a negative gate voltage to free the electrons trapped in the gate oxide.